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(71) Applicant: LEXMARK INTERNATIONAL, INC.
Lexington, Kentucky 40511 (US)

(72) Inventors:
- Parish, George Keith
Winchester, Kentucky 40391 (US)
- Steward, Lawrence Russell
Lexington, Kentucky 40517 (US)

(74) Representative: Tomlinson, Kerry John
Frank B. Dehn & Co.,
European Patent Attorneys,
179 Queen Victoria Street
London EC4V 4EL (GB)

(54) Ink jet print head identification circuit with serial out, dynamic shift registers

(57) An ink jet print head identification system for providing print head identifying information to the electronics of an ink jet printer includes one or more parallel load, serial out, dynamic shift registers (50 A-D) integrated into a print head chip having a plurality of address lines interconnecting the printer electronics and print head electronics. Each shift register is programmed or encoded with a single digital bit. In one embodiment, a voltage pulse (load signal) (70) received on a single chip address line by a plurality of shift registers (50 A-D) loads the input of each encoded register with the register's own encoded bit. Two of the address lines (72,74) provide each of the registers with successive sequential clock signals (1,2) to serially shift the encoded information to an output device (80) where the print head identifying information is read by the printer electronics. Other embodiments of the invention may employ any number of encoded registers independently of the number of available address lines.

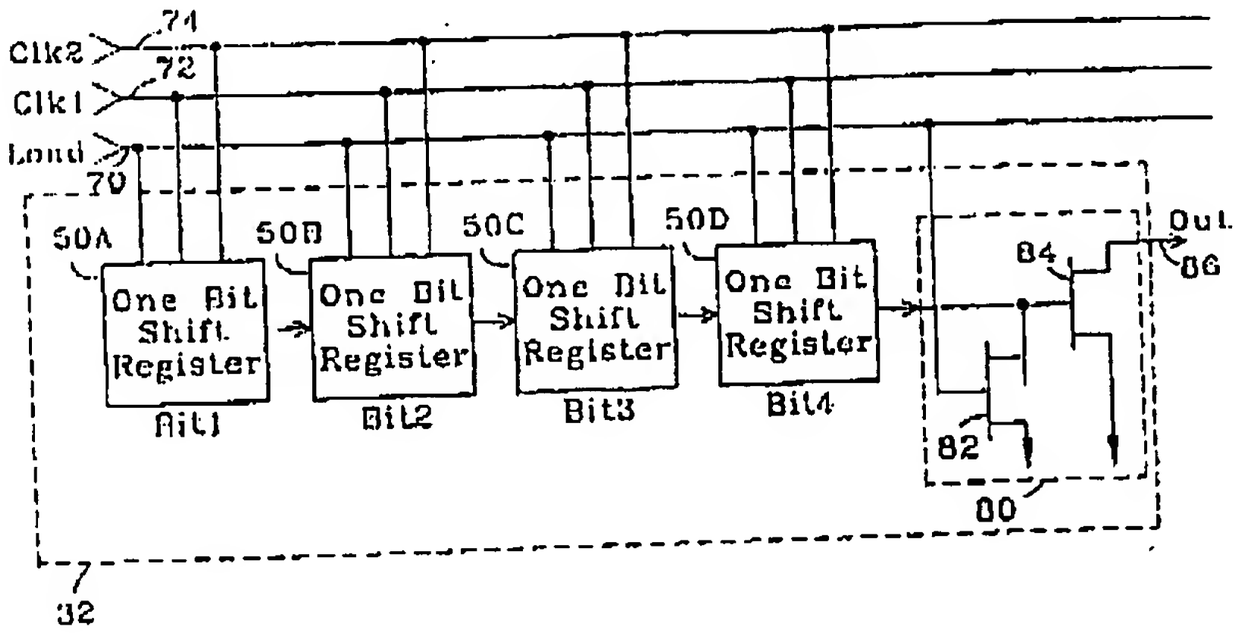

Fig. 3

Printed by Jouve, 75001 PARIS (FR)

Description

The present invention relates to an ink jet print head identification circuit and method.

Ink jet type printers employ a printing head that consists of a series of nozzles, or orifices, positioned in an orifice plate for expelling ink onto a printing surface. The ink can be expelled by a variety of means, including continuous, piezoelectric, and thermal/bubble jet. While several different ink jet technologies have evolved over the past two decades, the most popular ink jet technology today is the bubble jet where ink within a chamber is locally superheated to form an expanding bubble which propels a drop of ink through an orifice and onto the printing surface. Piezoelectric printers function in a similar manner inasmuch as ink is expelled through an orifice. However, instead of boiling the ink in a chamber, the ink is essentially squeezed from the chamber as a result of deflections/expansions generated by a piezoelectric ceramic transducer. The ceramic transducer changes its physical dimensions when subjected to an electric field, thereby generating a pressure wave within the ink chamber and expelling an amount of ink through the chamber orifice. Both piezoelectric and bubble-jet methodologies are considered "drop-on-demand" or "impulse" technologies, i.e., a drop of ink is ejected from the print head only when desired.

Each type of ink jet print technology requires its own unique type of print head, and print heads may further vary based on parameters such as whether the print head contains only black ink, or whether it is capable of color printing. Generally, the different types of print heads are interchangeable, except that most printers are unable to accommodate both black ink and color due to physical differences between the print heads, i.e., print heads designed for color printing are typically larger to accommodate a variety of ink colors. Other print head parameters include architecture, resolution, number of ink jet nozzles, and spacing between the nozzles. Because print heads are interchangeable, the printer electronics must know what particular type of print head is installed, as well as information relating to the various print head parameters, so that algorithms within the printer control system can be reconfigured to provide appropriately formatted print commands to the print head electronics.

Therefore, it is desirable to provide the printer electronics with information relating to the characteristics of the particular print head that is installed. This can be done by digitally encoding the identifying information into the print head electronics and enabling the printer electronics to retrieve that information as it is needed.

A number of attempts have been made in the prior art to provide print head identifying information to the printer electronics. U.S. Patent No. 4,872,027 to Buskirk et al. discloses providing extra electrical contact pads on the resistor network/array which fires the nozzles of the print head. These contact pads are selectively electrically connected in the resistor network to fire the individual nozzles in one of several unique configurations, each of which defines a specific print head. The code provided by these unique configurations of the electrical pads is detectable by the printer so that the type of head installed is determinable. This is accomplished by selectively connecting the individual electrical pads (or not connecting them) to the resistor circuits or circuit traces. By individually toggling the resistor lines at high or low voltage levels and detecting a voltage level shift on the lines associated with the extra contact pads, a connection (or lack thereof) may be detected.

Other prior art approaches to providing print head identifying information to the printer disclose identification circuitry disposed in the print head. U.S. Patent No. 4,930,915 to Kikuchi et al. discloses print head identification means disposed in a print head. In one embodiment, a 24-pin print head is identified when the printer electronics read a "high" state value on a signal line interconnecting the printer electronics and identification means. A 9-pin print head is identified by a "low" state signal. In another embodiment of the Kikuchi invention, a parallel-serial converter produces a predetermined identification signal.

U.S. Patent No. 5,363,134 to Barbehenn et al. discloses an integrated circuit for use in the print head of an ink jet printer. The integrated circuit includes an array circuit having a plurality of resistor cells arranged into rows and columns for heating an ink reservoir to produce a pattern of ink jets. A corresponding number of row and column lines are coupled to the array circuit for selecting and energizing the resistor cells according to the desired print pattern. An identification circuit is integrated into the same substrate as the array circuit. The identification circuit is programmable by means of a plurality of programmable paths corresponding and coupled to each row line. These programmable paths each include a programmable fuse and an active device connected in series. The opposite ends of the programmable paths are coupled together at a common node, which in turn is coupled to an output circuit for providing a single serial output signal in response to a sequential polling of the row lines.

The number of bits of identifying information that Barbehenn is capable of providing to the printer electronics is limited to the number of row lines available. For example, if there are a total of seven row lines interconnecting the array circuit with the printer electronics, then Barbehenn's identification circuit will be limited to storing seven and only seven bits of identifying information because each of the programmable paths correspond with and are coupled to a unique one of the row lines. To provide an identification circuit that contains greater than seven bits of identifying information, Barbehenn would be required to increase the number of row lines, or address lines available.

Thus, there is a need for an efficient, inexpensive, print head identification circuit that preferably is not lim-

ited by the number of address lines interconnecting the existing print head electronics and printer electronics.

The present invention provides an identification system for providing ink jet print head identifying information in ink jet printers having ink jet print heads. The system includes a controller and drive circuit for transmitting signals including at least one clock signal in the form of clock pulses. The controller and drive circuit also receive signals. A plurality of address lines are provided for transmitting signals, including the at least one clock signal, from the controller and drive circuit to the ink jet print head. An identification circuit disposed in the ink jet print head contains a digital code corresponding to the print head identifying information. The identification circuit is connected to receive the at least one clock signal from the address lines and is responsive to the at least one clock signal to serially transmit the digital code. An output line is connected to the identification circuit for transmitting the bits of the digital code to the controller. The controller is connected to receive the bits of the digital code from the output line, and programmed to interpret the digital code and determine the print head identifying information.

The identification system may further include a temperature sense circuit connected to the output line for transmitting information corresponding to the temperature of the print head.

An example of the identification circuit includes a predetermined number of shift registers. Each of these shift registers is programmed in accordance with the digital code to produce an output of either a logic one or a logic zero in response to the at least one clock signal.

The controller and drive circuit may be configured to transmit at least one load signal on the address lines. When so configured, the identification circuit includes a predetermined number of shift registers where each shift register is programmed in accordance with the digital code to produce an output of either a logical one or a logical zero in response to the at least one load signal and the at least one clock signal. The controller is programmed to transmit the load signal and, following the load signal transmission, to interpret a next predetermined number of bits on the output line as the digital code.

The controller and drive circuit may also be configured to transmit at least one load signal and first and second clock signals on the address lines. In such a case, the identification circuit includes a load circuit and a transmit circuit. The load circuit is connected to receive the load signal from the address lines, and is responsive to the load signal to load the digital code into the transmit circuit as the loaded digital code. The transmit circuit is responsive to the loaded digital code and the first and second clock signals to serially transmit the digital code on the output line. The controller is programmed to transmit the load signal and, following the load signal transmission, to interpret a next predetermined number of bits on the output line as the digital code.

In another embodiment of the present invention, an ink jet print head identification circuit is integrated into an ink jet print head chip having print head electronics, a plurality of address lines, and a print head temperature sense circuit with an output. The identification circuit provides print head identifying information to an ink jet printer and includes an output device and a plurality of programmed one bit shift registers. The shift registers are interconnected to the address lines and the output device for serially shifting the programmed contents of the registers to the output device in response to signals received on the address lines.

The signals may, for example, include at least one clock signal and a load signal. In this example, the registers are interconnected to each other to serially shift their programmed contents to the output device in response to the at least one clock signal and the load signal.

As an example of the output device, there is an output transistor having a source, drain, and gate. The gate of the output transistor receives the serially shifted, programmed contents of the shift registers. A pull up device pulls up the signal level on the drain of the output transistor. The programmed contents of the shift registers are received by the output transistor. A discharge device discharges parasitic capacitance at the gate of the output transistor following reception of the programmed contents.

Another preferred embodiment of the present invention is disclosed where an ink jet print head integrated circuit provides print head identifying information to ink jet printer electronics. The integrated circuit includes a print head array circuit.

A plurality of address lines are connected for transmitting signals from the printer electronics to the print head array circuit. The address lines include lines for conveying first and second clock signals and a line for conveying a load signal. A temperature sense circuit having an output is connected to the printer electronics. A programmed identification circuit is connected to receive the first and second clock signals and the load signal. The identification circuit also provides print head identifying information to the temperature sense circuit output in serial digital format in response to the first and second clock signals and the load signal.

An example of the identification circuit for this embodiment includes a load circuit and a transmit circuit. The load circuit is connected to receive the load signal from the address lines and is responsive to the load signal to load the identifying information into the transmit circuit. The transmit circuit is responsive to the loaded identifying information and the first and second clock signals to serially transmit the loaded identifying information on the temperature sense circuit output.

The present invention also discloses a method for providing ink jet print head identifying information to an ink jet printer having printer electronics and an ink jet print head. The print head includes an integrated circuit

having print head array electronics, a temperature sense circuit with an output connected to the printer electronics, an identification circuit, an output device connected to the temperature sense circuit output, and a plurality of address lines interconnecting the identification circuit and printer electronics. The method includes the steps of programming a digital code having one or more bits into the identification circuit. Each bit of the code is programmed as either an electrically conducting short or a non-conducting gap, where the digital code corresponds to the print head identifying information. Signals generated by the printer electronics, including at least one clock signal in the form of clock pulses, are transmitted on the address lines to the identification circuit. One or more bits of the digital code are transmitted to the output device in serial digital format in response to the signals generated by the printer electronics. The digital code is read by the printer electronics as it is transmitted to the output device.

The method may further include the step of determining the identifying information from the transmitted digital code by the printer electronics based in part on the condition of each bit as either a gap or a short.

The method may also include the step of transmitting a load signal, as a printer electronics signal, to the identification circuit via the address lines.

As another additional step in the method, the output device may be reset following transmission of the digital code to the output device.

Certain preferred embodiments of the invention will now be described by way of example and with reference to the drawings wherein like reference characters designate like or similar elements throughout the several drawings as follows:

FIG. 1 is a block diagram of the print head identification system;
FIG. 2 is a circuit diagram of a one bit dynamic shift register;
FIG. 3 is a block diagram of a four bit, parallel in, serial out identification circuit; and FIG. 4 is a timing chart for the circuit of FIG. 3.

There is shown in FIG. 1 a block diagram of an ink jet print head identification system 20 including ink jet printer electronics 22 and ink jet print head electronics 24. Typically, bubble jet print heads incorporate a resistor array, or print head array 30 for selectively boiling and expelling ink through orifices in an orifice plate (not shown) on the print head. Resistors within the array 30 are selectively energized through appropriate signals received from the printer electronics 22 on address lines 29. Within the printer electronics 22 a microprocessor controller 26, which is typically an ASIC controller providing TTL level outputs, sends print data commands to a head drive circuit 28. In a preferred embodiment, the drive circuit 28 is a TEXAS INSTRUMENTS 75373, 100 milliamp, push-pull driver.

Drive circuit 28 converts print data commands received from the controller 26 into appropriately formatted analog pulses which are demultiplexed and sequentially provided to the print head electronics 24 via address lines 29. These analog pulses possess sufficient intensity to heat the resistors within the print head array 30 so that ink within the print head boils to form a bubble, thereby expelling ink through an orifice. The number of address lines 29 available will vary depending on the particular printer that is used.

Because different styles and types of ink jet print heads requiring differently formatted analog pulses are interchangeable in ink jet printers, it is important for the printer electronics 22 to possess information relating to the print head that is installed in the printer. Print head parametric information is useful to the printer electronics 22 because it allows the printer electronics 22 to reconfigure print control algorithms to produce analog pulses that are appropriate for the specific print head installed. The present invention provides print head identifying information to the printer electronics 22 by encoding the information digitally in an identification (ID) circuit 32 that is integrated into the print head electronics 24 during fabrication.

Typically, print head electronics 24 are fabricated as a single integrated chip. In addition to the print head resistor array 30 and corresponding address line connections 29, the chip will normally incorporate a temperature sense circuit 34. The temperature sense circuit 34 is typically a metal resistor that senses the temperature of the print head during printing. The sensed temperature is provided as an analog signal to the printer controller 26 on output line 35, enabling the printer controller 26 to monitor the print head for overheat conditions.

To reduce I/O requirements, the ID circuit 32 of the present invention uses some, but not all, of the existing address lines 29 for receiving inputs from the printer electronics 22 and it uses the existing temperature sense output 35 to serially transmit the encoded print head identifying information to the printer electronics 22. A maximum of three address lines are used by the ID circuit 32 to receive inputs, and the number of encoded bits of information within the ID circuit 32 is independent of the number of address lines 29 used. There is minimal or no interference with the temperature sense output 35 during normal operation because the printer electronics 22 will read temperature sense only when the printer is idle.

In a preferred embodiment, print head identifying information is digitally encoded into the ID circuit 32 by means of one or more programmed, one bit dynamic shift registers 50 such as the one shown in FIG. 2. The shift register 50 is, for example, mask programmed during fabrication by either connecting the source of load transistor 52 to ground 51 to produce a logic "0" when the gate of load transistor 52 is made active by a load signal 70 received on one of the address lines 29, or by connecting the source of load transistor 52 to a voltage

source 53 to produce a logic "1" when the gate of load transistor 52 is active. When the gate of load transistor 52 becomes active by load signal 70, the programmed logic, or voltage level is passed to the gate of input transistor 54. After transistor 52 turns off, the passed voltage level will remain stored in the parasitic gate capacitance of input transistor 54. Because the voltage at the gate of input transistor 54 will eventually discharge due to leakage currents, the voltage is considered dynamically stored on the gate.

With the input 78 loaded with the programmed voltage level, it can now be shifted to the output 76. This is accomplished by sequential clock signals transmitted by the printer electronics 22 and received by the shift register 50. A clock 1 input is received on line 72 and a clock 2 input is received on line 74, where each clock input 72, 74 is received from the printer electronics 22 via a separate address line 29. A voltage pulse on the clock 1 input 72 passes the logical inverse from the gate of input transistor 54 to the gate of output transistor 60. When the clock 1 input 72 is active, load transistor 56 turns on as does pass transistor 58. If the input 78 of the shift register 50 is a logic "1", input transistor 54 will turn on and the gate of output transistor 60 will discharge. If the input 78 of the shift register 50 is a logic "0", input transistor 54 will remain off and the gate of output transistor 60 will be charged through load transistor 56 and pass transistor 58. When the voltage pulse on the clock 1 input 72 goes inactive, pass transistor 58 turns off and the voltage level (i.e., the logic inverse of the voltage level that was parasitically stored on the gate of input transistor 54) will be dynamically stored on the gate of output transistor 60.

A voltage pulse on the clock 2 input 74 passes the logic inverse from the gate of output transistor 60 to the output 76 of the shift register. When the clock 2 pulse is active, load transistor 62 turns on as does pass transistor 64. The logic inverse of the gate voltage on output transistor 60 passes to the output 76 of the shift register. Therefore, after successive pulses on the clock 1 and 2 inputs 72, 74, the logic level on input 78 is passed to the output 76 as a single bit.

It should be noted that, because the load transistors 52, 56, 62 are off at all times except during clock pulses, the register 50 of FIG. 2 consumes little power.

In a preferred embodiment, several shift registers 50 are connected in series to provide a digital code, such as the four bit example shown in FIG. 3. A voltage pulse on load signal 70 initiates a parallel load of the encoded logic level, or bit encoded within each of the four shift registers 50A-D. As previously discussed, this results in the programmed logic level being dynamically stored at the input 78 (FIG. 2) of each shift register 50A-D. A pulse on the clock 1 input 72 followed by a pulse on the clock 2 input 74 shifts the logic level from each register input 78 to each register output 76 so that each register output 76 is dynamically stored on the input 78 of the next register.

With each clock 1 and clock 2 sequence of pulses, each programmed bit is successively and serially shifted to an output device 80 and read by the controller 26 until all bits have been read by the controller 26. The controller 26 is programmed to interpret the code and determine the print head identifying information and reconfigure print control algorithms accordingly. In this manner, a single ink jet printer is able to accommodate many different types of print heads.

As shown in FIG. 3, the output device 80 preferably includes an open drain output transistor 84 and a discharge transistor 82. The voltage level at the drain of output transistor 84 is pulled up on line 86 through a load device (not shown) within the printer electronics 22 (FIG. 1) so that the printer controller 26 reads a programmed logic level after each clock 2 pulse. For example, when a clock 2 pulse causes a programmed logic level "1" to be transmitted to the gate of output transistor 84, output transistor 84 will become active and the drain will be pulled down. The controller 26 detects the lowered voltage level at the drain by reading the voltage level at line 86 and thereby senses that a logic level "1" has been transmitted by the ID circuit 32. Similarly, with each successive clock 2 pulse the programmed logic levels of the shift registers 50A-D are sequentially shifted and serially transmitted to output transistor 84 to be read by the controller 26. FIG. 4 is a timing chart for serial transmission of four bits of encoded information by the ID circuit 32 of FIG. 3.

With continued reference to FIG. 3, the open drain output 86 preferably utilizes an existing chip I/O line to serially transmit the encoded identifying information to the printer controller 26, such as the temperature sense output 35. Utilization of the existing temperature sense output 35, along with the fact that the encoded information is serially transmitted, eliminates the need for additional chip output lines. After all bits of the encoded information have been read, a pulse on the load signal line 70 activates discharge transistor 82 to discharge the gate of output transistor 84, thereby enabling valid temperature sense information to be transmitted to the controller 26 immediately after the gate of output transistor 84 has been discharged. To prevent possible interference with normal operation of the temperature sense circuit 34, a pulse is output by the controller 26 on the load signal line 70 prior to each read of the temperature sense circuit 34. This ensures that the gate of output transistor 84 remains discharged during temperature control operations.

The controller 26 reads the serial digital output on line 86 and determines print head identifying information by comparing the received bit pattern against stored correlations of print head information. With the print head properly identified by the printer controller 26, the controller 26 is now able to reconfigure its control system algorithms to accommodate printing with the installed print head.

It will be understood that any number of shift regis-

ters 50 may be employed in the present invention without increasing the required number of address lines 29. Therefore, there is disclosed an ink jet print head identification circuit 32 for serially transmitting to the printer controller 26 a digital code containing print head identifying information where the number of bits comprising the digital code is independent of the total number of address lines 29 available.

It is contemplated, and will be apparent to those skilled in the art from the foregoing specification and drawings that modifications and/or changes may be made in the embodiments of the invention. Accordingly, it is expressly intended that the foregoing are illustrative of preferred embodiments only, not limiting thereto, and that the true scope of the present invention be determined by reference to the appended claims.

Claims

1. An ink jet print head (24) containing ink, characterised by:

   an identification circuit (32) disposed in the ink jet print head (24) and containing a digital code corresponding to print head identifying information;
   an input line connected to said identification circuit, said identification circuit thereby receiving control signals (29) and being responsive to the control signals (29) to serially transmit the digital code; and
   an output line (35) for interconnecting said identification circuit (32) and a printer for conducting the digital code when transmitted to provide the print head identifying information as an output.

2. The apparatus of claim 1 wherein said identification circuit (32) is further characterized as including a plurality of programmed one bit shift registers (50A-50D) for serially shifting the programmed contents of the registers to the output line in response to control signals (29).

3. The apparatus of claim 2 wherein said identification circuit (32) is further characterized as including an output device (80) that serially holds and transmits a bit of the digital code on said output line.

4. The apparatus of claim 2 wherein said control signals (29) are characterized as shift signals including at least one clock signal (72) and at least one load signal (70).

5. The apparatus of claim 1 wherein said output line (35) is further characterized as the output of a print head temperature sensing device (34).

6. The apparatus of claim 1 wherein said ink jet print head (24) is further characterized as an ink jet print head (24) for depositing, onto a print medium, ink having parameters corresponding to the print head identifying information.

7. The apparatus of claim 6 wherein said output device (80) is further characterized by:

   an output transistor (84) having a source, drain, and gate, said gate connected to serially receive and transmit the digital code;
   a pull up device for pulling up the signal level on the drain of the output transistor (84), said digital code being reflected in the signal level at the drain as the digital code is received by the output transistor (84), and
   a discharge device (82) for discharging parasitic capacitance at the gate of the output transistor (84) following reception of the digital code.

8. The apparatus of claim 1 wherein said print head identifying information identifies parameters of the ink jet print head (24) including ink color.

9. An ink jet print apparatus (20) for providing print head identifying information to an ink jet printer, said apparatus characterized by:

   a printer control circuit (26) for producing control signals;
   a plurality of address lines (29) for conducting said control signals;
   an ink jet print head (24);
   ink contained in said print head (24);
   an identification circuit (32) disposed in the ink jet print head (24) and containing a digital code corresponding to the print head identifying information, being connected to said address lines (29) to receive the control signals from the printer's control circuit (26) and being responsive to the control signals to serially transmit the digital code to the printer control circuit (26); and
   an output line (35) interconnecting said identification circuit (32) and said printer control circuit (26) for conducting the digital code to the printer control circuit (26);
   wherein said printer control circuit (26) interprets the digital code and determines the print head identifying information.

10. The apparatus of claim 9 wherein said identification circuit (32) is further characterized as including a plurality of shift registers (50A-50D).

11. The apparatus of claim 10 wherein said print head identifying information identifies parameters of the

ink jet print head (24) including ink parameters.

12. The apparatus of claim 1 wherein said ink parameters are further characterized as colors.

13. A method for providing, to an ink jet printer, identifying information which identifies the type of ink jet print head (24) that deposits, onto a print medium, ink having parameters corresponding to the identifying information, the method characterized by the steps of:

attaching an ink jet print head (24) containing ink to an ink jet printer;
programming a digital code into an identification circuit (32) disposed on the print head (24), each bit of the digital code being programmed as either an electrically conducting short or a non-conducting gap, the digital code corresponding to the print head identifying information;
transmitting control signals (29) generated by the printer to the identification circuit (32);
transmitting one or more bits of the digital code to an output device 80 in serial digital format in response to the control signals (29); and
reading the digital code by the printer as the digital code is transmitted by the output device (80).

14. The method of claim 13, further characterized by the step of resetting the output device (80) following transmission of the digital code to the output device (80).

15. The method of claim 13, further characterized by the step of interpreting the digital code by the printer to identify parameters of the print head including ink parameters.

16. The method of claim 13, further characterized by the step of interpreting the digital code by the printer to identify the color of the ink.

17. A method for providing, to an ink jet printer, information which identifies an ink jet print head (24) that deposits, onto a print medium, ink having parameters corresponding to the identifying information, the method characterized by the steps of:

attaching an ink jet print head (24) to an ink jet printer; providing ink to the print head (24);
programming a digital code into an identification circuit (32) disposed on the print head (24), each bit of the digital code being programmed as either an electrically conducting short or a non-conducting gap in a plurality of shift registers (50A-50D), the digital code corresponding to the print head identifying information;
transmitting control signals (29) generated by the printer to the identification circuit (32);
transmitting one or more bits of the digital code to an output device (80) in serial digital format in response to the control signals (29);
reading the digital code by the printer as the digital code is transmitted to the output device (80); and
identifying the type of print head (24) and ink based on the print head identifying information.

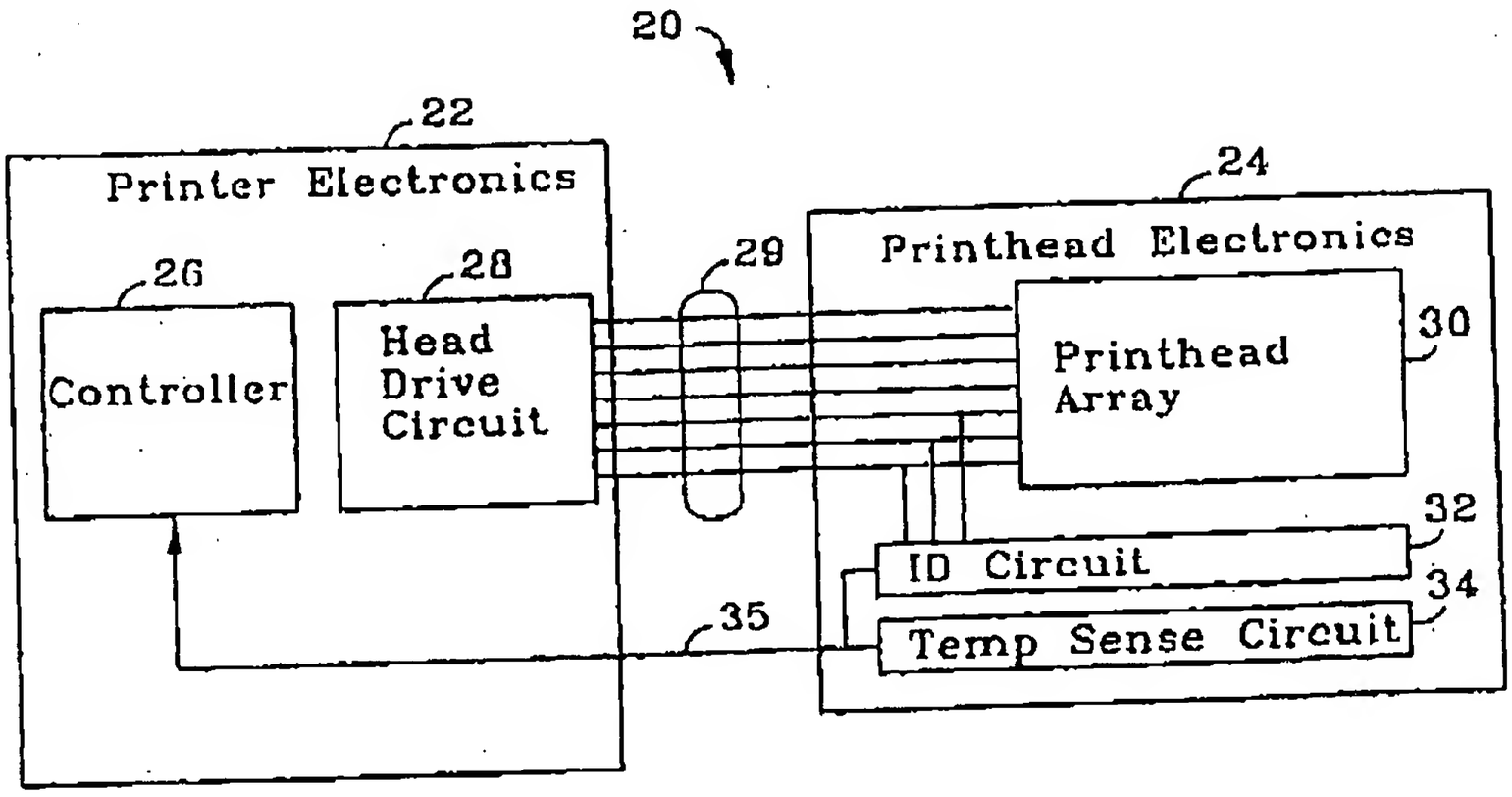

Fig. 1

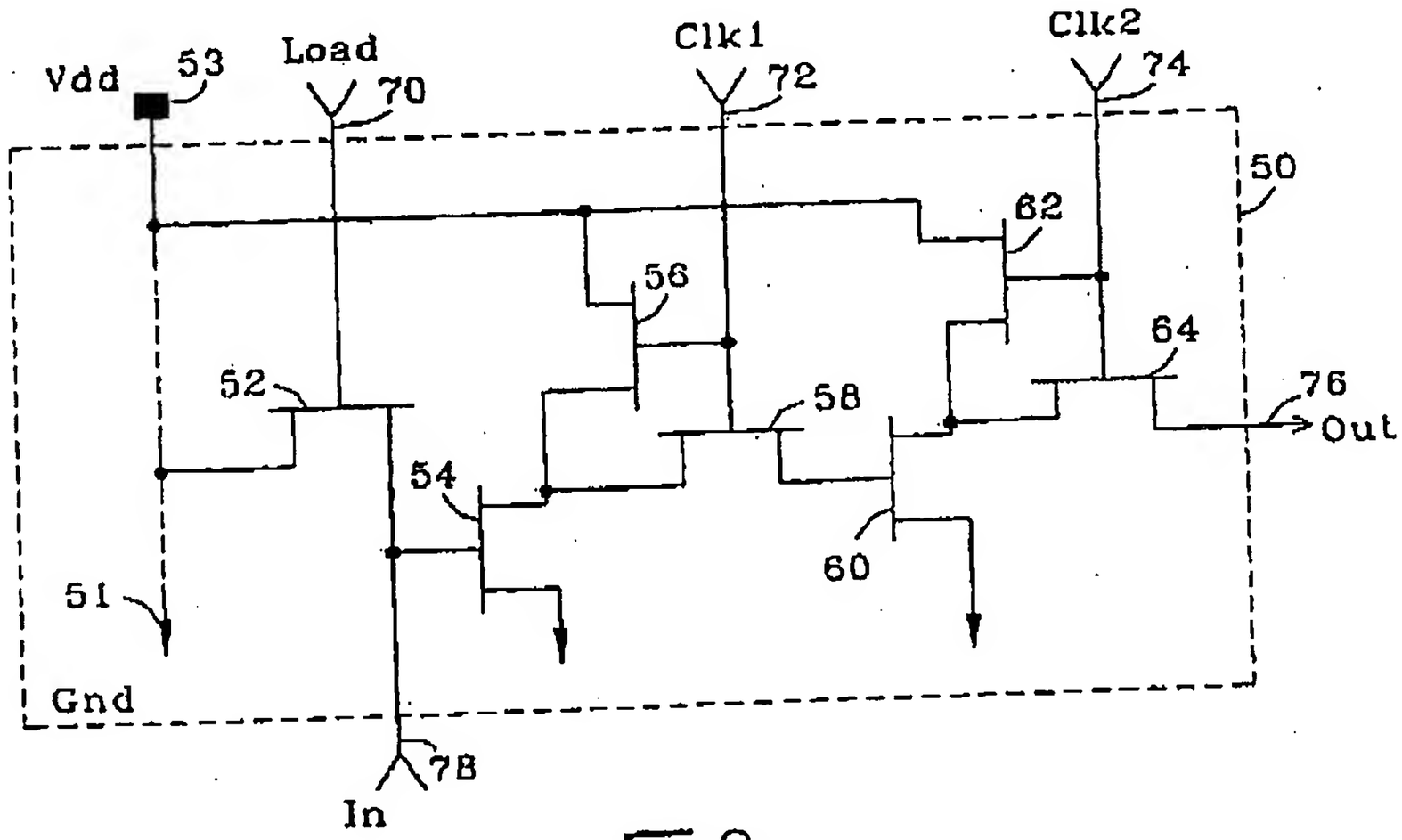

Fig. 2

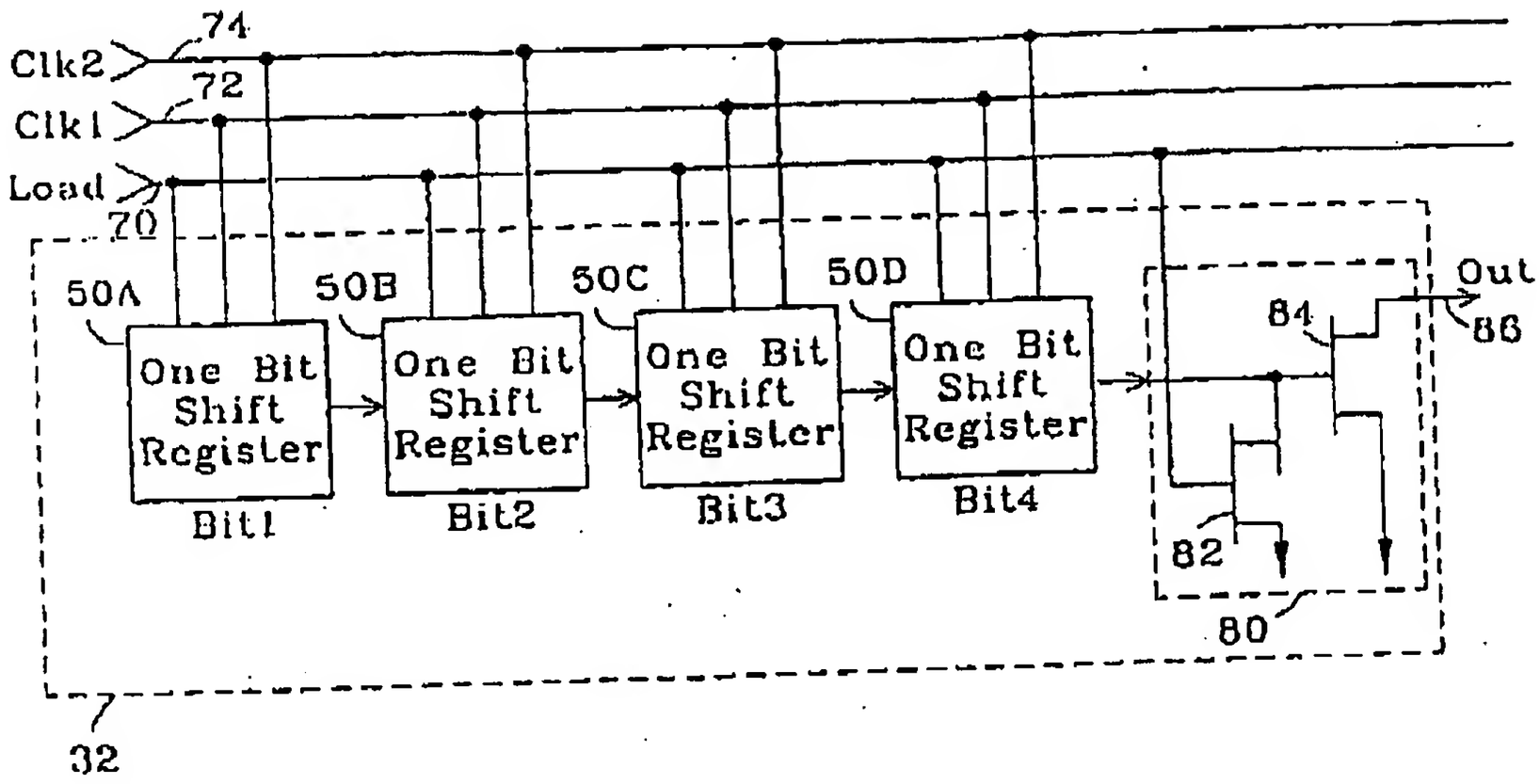

Fig. 3

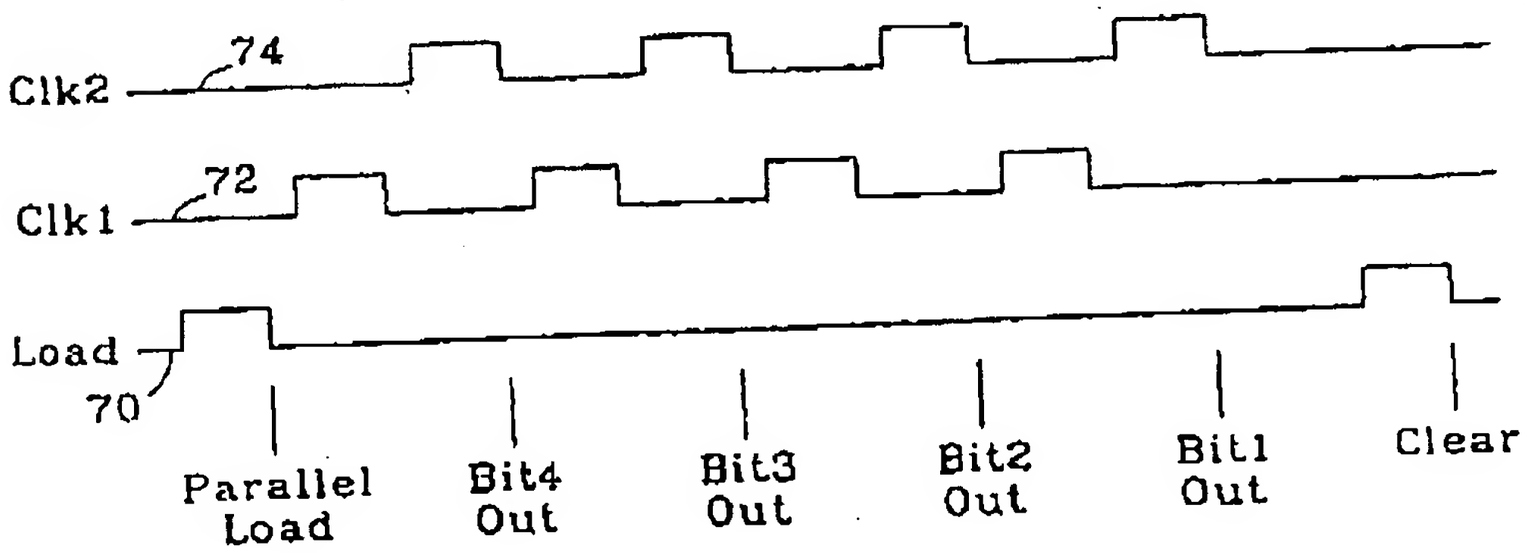

Fig. 4

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EUROPEAN SEARCH REPORT

Application Number
EP 96 30 7123

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,X	EP-A-0 571 093 (HEWLETT-PACKARD COMPANY) * column 7, line 49 - line 53 *	1-17	B41J25/34
D,X	EP-A-0 315 417 (HEWLETT-PACKARD COMPANY) * claim 8 *	1	
A	EP-A-0 541 064 (EASTMAN KODAK COMPANY) * claim 2 *	1-17	
A	US-A-5 049 898 (ARTHUR ET AL.) * column 2, line 14 - line 32 *	1-17	
A	US-A-5 289 210 (TAKAYANAGI) * column 4, line 48 - line 59 *	1-17	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			B41J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 December 1996	Joosting, T

CATEGORY OF CITED DOCUMENTS

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